Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.087”**

**ANODE**

**.087”**

**Top Material: Ni/Au**

**Backside Material: Ni/Au**

**Bond Pad Size: .011 X .011”**

**Backside Potential: CATHODE**

**Mask Ref: CPD25**

**APPROVED BY: DK DIE SIZE .087” X .087” DATE: 2/27/23**

**MFG: CENTRAL SEMI THICKNESS .011” P/N: 1N5417**

**DG 10.1.2**

#### Rev B, 7/1